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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/772,920

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Lawrence A. Clevenger

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10/23/2002

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EXAMINER

KESHAVAN, BELUR V

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/772,920

Applicant(s)

CLEVINGER ET AL.

Examiner

Belur V Keshavan

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) 1-17 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 January 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-16 are drawn to a method of forming an interconnect on a semiconductor device substrate, classified in class 438, subclass 629.
- II. Claim 17 is drawn to a semiconductor device, classified in class 257, subclass 774.

The inventions are distinct, each from the other because of the following reasons:

Inventions of Group I and Group II are related as process of making and product made respectively. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the device of Group II can be made by forming relatively narrow structures first in a dielectric and then converting a relatively narrow structure into a relatively wide structure.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Sean M. McGinn on 09/30/2002 a provisional election was made ^{w/o traverse} with traverse to prosecute the invention of Group I, claim 1-16. Affirmation of this election must be made by applicant in replying to this Office action. Claim 17 is

Art Unit: 2825

withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

In claims 5 and 13, selectively removing the conductive material is not shown in the drawings and must be shown in the drawings or the feature canceled from the claim. No new matter should be entered.

In claim 15, the subsequent dielectric films and metal layers on the resulting structure as claimed in claim 15, must be shown in drawings or the feature(s) canceled from the claim(s). No new matter should be entered.

Proposed drawing correction or corrected drawings are required in reply to the Office Action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 6 is objected to because of the following informalities: In claim 6, the terms "TEOS and silane" are used to claim the type of dielectric used where as TEOS and silane are reactive gases and are not dielectrics. Examiner suggests using the terms TEOS oxide and silane oxide instead. Appropriate correction is required.

Art Unit: 2825

Any further indication of rejection of, or indication of allowance of, claim 6 is based on claim 6 as it is understood by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as Claim 10 recites the limitation "the relatively small contacts" in claim 5 and there is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 8, 9, 12-14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shoda (U. S. Patent No. 5,529,953).

Regarding claims 1, 2 and 3 Shoda discloses, in columns 3-5 and in figures, 1a-1e a method of forming an interconnect on a semiconductor substrate comprising:

Forming relatively narrow first structure (3) and forming a relatively wider second structure (4) in a dielectric (2) formed on a semiconductor substrate (1);

Forming a liner comprising a CVD metal and a metallization over the liner (7, 8, and W) in the first and the second structures such that the first structure is filled first and then the second structure is filled after the first structure is filled.

Regarding claims 5, 8, 9, 12, 13, 14 and 16 Shoda discloses a method of forming interconnect on a semiconductor substrate with semiconductor devices such as DRAM with a first level of metallization comprising:

Forming a contact (5) including slot (3) in a dielectric (2) formed on a semiconductor substrate (1);

Forming troughs (9) between the first and the second level metals including a slot (3) into the dielectric thereby to form a dual damascene structure (figure 7);

Depositing a conducting material (8) comprising CVD tungsten on the dielectric;

Depositing a metal (W) over the conducting material to completely fill the slot and the trough

Removing the metal by CMP either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric and selectively removing the conductive material comprising selective etch or selective CMP in column 4 and lines 55-62.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering Patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoda in view of Liu et al. (U. S. Patent No. 6,284,642 B1).

Regarding claims 4 and 11, Shoda anticipates claims 1 and 5 respectively as given above but lacks metallization comprising copper. Liu et al. teach in column 7 and lines 34-38 the use of copper for metallization in dual damascene interconnection structures in the production of semiconductor devices. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Shoda with that of Liu et al. and use copper for metallization in dual damascene interconnection structures in the production of semiconductor devices. The rationale behind combining the teachings is to have low resistance reliable interconnections with simple manufacturing techniques.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoda in view of S. Wolf (Silicon Processing for the VLSI Era, Vol. 2, p 194)

Regarding claim 6, Shoda anticipates claim 5 as given above but lacks TEOS oxide. In the art the use of TEOS oxide in multilevel interconnection is notoriously very well known. S.

Art Unit: 2825

Wolf teaches on page 194 the use of TEOS oxide in multilevel interconnection. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Shoda with that of S. Wolf and use TEOS oxide as the dielectric. The reasons for this combination is that TEOS oxide can be deposited at relatively low temperature within the thermal budget and is very amenable for dual damascene process.

Regarding claim 7, shoda discloses, in column 3, lines 40-45, forming a contact (5) wherein contact comprises contact formed between the first metal level and the second metal level formed on the semiconductor.

Regarding claim 15. Shoda anticipates claim 5 as above but lack subsequent dielectric films and metal layers on the resulting structure. Shoda teaches in greater details of depositing dielectric film and metal layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the deposition of dielectric films and metal layers on the resulting structure, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, USPQ 8.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 703 306 5985. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703 308 1323. The fax phone numbers for the

Art Unit: 2825

organization where this application or proceeding is assigned are 703- 872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

Bvk ~~VSK~~
October 15, 2002.

Belur V. Keshavan
Examiner. Art Unit 2825.



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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